



180 MS/s 16-Bit PCI Express Digitizer

2 channels sampled at 16-bit resolution
 180 MS/s simultaneous real-time sampling rate on each input
 ±200mV to ±16V input range
 FIFO streaming mode

Dual DMA engines
 AlazarDSO oscilloscope software
 Software Development Kit supports C/C++, C#, VB and LabVIEW

Overview

ATS9462 is a 4-lane PCI Express (PCIe x4), dual-channel, high resolution, 16 bit, 180 MS/s waveform digitizer card capable of streaming acquired data to PC memory at rates up to 720 MB/s. ATS9462 does not have any on-board acquisition memory.

Users can capture data from one trigger or a burst of triggers. Users can also stream very large datasets continuously to PC memory or hard disk.

ATS9462 allows users to build real-time data acquisition systems even under the Windows or Linux operating systems, as users are allowed to read acquired data even while the next acquisition is in progress.

ATS9462 PCI digitizers are an ideal solution for cost sensitive OEM applications that require a digitizer to

be embedded into the customer’s equipment.

ATS9462 is supplied with AlazarDSO software that lets the user get started immediately without having to go through a software development process.

Users who need to integrate the ATS9462 in their own program can purchase a software development kit, ATS-SDK for C/C++ and VB, or ATS-VI for LabVIEW for Windows or a Linux based ATS-Linux.

All of this advanced functionality is packaged in a low power, half-length PCI Express card.

Product	Bus	Operating System	Channels	Sampling Rate
ATS9462	PCIe x4	Windows 2K/XP, Vista, Linux 2.6	2	180 MS/s to 1



PCI Express Bus Interface

ATS9462 interfaces to the host computer using a 4-lane PCI Express bus. Each lane operates at 2.5 Gbps. PCIe bus specification v1.0a and v1.1 are supported.

According to PCI specification, a 4-lane board can be plugged into any 4-lane, 8-lane or 16-lane slot, but not into a 1-lane slot. As such, ATS9462 requires at least one free 4-lane, 8-lane or 16-lane slot on the motherboard.

The physical and logical PCIe x4 interface is provided by an on-board FPGA, which also integrates acquisition control functions, memory management functions and acquisition datapath. This very high degree of integration allows for optimum product reliability.

PCI Express is a relatively new bus and, as such, throughput performance may vary from motherboard to motherboard. AlazarTech's 720 MB/s benchmarks were done using a Dell Precision 390 workstation that uses the server-class Intel 955X Express chipset.

At the time of release of ATS9462, desktop-class PCI

Express chipsets, such as the Intel G965 Express, provided data throughput closer to 400 MB/s.

Users must always be wary of throughput specifications from manufacturers of waveform digitizers.

Some unscrupulous manufacturers tend to specify the raw, burst-mode throughput of the bus. AlazarTech, on the other hand, specifies the benchmarked sustained throughput. To achieve such high throughput, a great deal of proprietary memory management logic and kernel mode drivers have been designed.

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PCI Digitizers

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Analog Input

An ATS9462 features two analog input channels with extensive functionality. Each channel has 65 MHz of full power analog input bandwidth. With software selectable attenuation, you can achieve an input voltage range of $\pm 200\text{mV}$ to $\pm 16\text{V}$. Attenuating probes (sold separately) can extend the voltage range even higher.

Software selectable AC or DC coupling further increases the signal measurement capability. Software selectable 50Ω input impedance makes it easy to interface to high speed RF signals.

For applications that require the best signal integrity, an Amplifier Bypass Mode is available as a standard feature. This feature increases the SNR to 75 dB, increases input bandwidth to 85 MHz while leaving the input range fixed at a nominal value of $\pm 550\text{mV}$.

Acquisition System

ATS9462 PCI digitizers use a pair of state of the art 180MS/s, 16-bit ADCs to digitize the input signals. The real-time sampling rate ranges from 180 MS/s down to 1 KS/s. The two channels are guaranteed to be simultaneous, as they share the exact same clock.

An acquisition can consist of multiple records, with each record being captured as a result of one trigger event. A record can only contain post-trigger data.

Infinite number of triggers can be captured by ATS9462.

In between the multiple triggers being captured, the acquisition system is re-armed by the hardware within 32 sampling clock cycles.

This mode of capture, sometimes referred to as Multiple Record, is very useful for capturing data in applications with a very rapid or unpredictable trigger rate. Examples of such applications include medical imaging, ultrasonic testing, OCT and NMR spectroscopy.

On-Board Acquisition Memory

There is no on-board acquisition memory on the ATS9462.

PC memory is used for data storage, thanks to the on-board FIFOs and AlazarTech's advanced DMA engines.

FIFO Streaming Mode

A FIFO-based streaming mode is used on the ATS9462. This mode allows the operation of the board without any on-board acquisition memory.

FIFO streaming can work for both single record and multiple record acquisitions. The only restrictions are that there can be no pre-trigger acquisition, no time-stamping and no buffer headers.

It is also possible to stream a very long, gapless dataset using the on-board FIFOs.

In short, FIFO Streaming Mode has been designed for scanning applications such as OCT, ultrasonic inspection, radar and lidar.

FPGA Customization

A number of OEM applications require real-time signal processing of the digitized data. ATS9462 contains a large FPGA (Altera EP2SGX60) that is only 65% full. There are ample resources, including hardware multipliers, to implement FIR filters, demodulation, IQ detection, DDC, FFT etc.

All customization work has to be done at AlazarTech factory. Contact the factory to discuss your specific needs.

Software Selectable Bandwidth Limit

A majority of applications for PCI digitizers require oversampling of input signal, i.e. the frequency of the analog signal being digitized is a factor of 5 or 6 lower than the sample rate or even the Nyquist rate.

ATS9462 features a software-controlled bandwidth limit switch, which reduces high frequency noise and improves signal to noise ratio. This switch is independently selectable for each input channel.

When selected, bandwidth limit switch can reduce the input bandwidth of a particular input to be approximately 20 MHz.

Natural Input Range

A waveform digitizer provides the best dynamic performance when it is operated within its Natural Input Range (NIR). The NIR of a digitizer is defined as the input range for which the input signal has the minimum amount of gain or attenuation.

Minimum gain ensures that there is a minimum amount of noise that is injected into the signal due to amplification. Minimum attenuation ensures that the ratio between the signal amplitude and the ground noise is the highest.

NIR for the ATS9462 is the ± 800 Volt input range.

Amplifier Bypass Mode

To obtain optimum dynamic performance, choose the Amplifier Bypass Mode. This mode comes standard with the ATS9462.

Each channel can be independently bypassed using on-board DIP-switches.

Once the amplifier has been bypassed, the input for that channel has 50 Ω impedance, DC coupling and a 550 mV full scale input range. Diode protection is still included, but users should avoid saturation of the input beyond 120% of full scale

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Triggering

operand.

The user can specify the number of records to capture in an acquisition, the length of each record and the amount of pre-trigger data.

A programmable trigger delay can also be set by the user. This is very useful for capturing the signal of interest in a pulse-echo application, such as ultra-sound, radar, lidar etc.

Timebase

lato: a 10 MHz TCXO that is multiplied to produce the 180 MHz and 160 MHz sampling rate; a 125 MHz crystal oscillator provides the 125 MS/s sample rate; and a 100 MHz crystal oscillator that provides 100 MS/s and lower sampling rates.

Optional External Clock

While the ATS9462 features low jitter, high reliability

The ATS9462 is equipped with sophisticated digital triggering options, such as programmable trigger thresholds and slope on any of the input channels or the External Trigger input.

While most oscilloscopes offer only one trigger engine, ATS9462 offers two trigger engines (called Engines X and Y). This allows the user to combine the two engines using a logical OR, AND or XOR

Timebase on the ATS9462 can be controlled either by on-board clock sources or by optional External Clock.

On-board clock sources consist of three different oscil-

125MHz and 100MHz crystal oscillators and a 10MHz TCXO as the source of the time base system, there may be occasions when digitizing has to be synchronized to an external clock source.

ATS9462 External Clock option provides an SMA input for an external clock signal, which can be a sine wave or LVTTTL signal.

A new sample is taken by the on-board ADCs for each rising (or falling) edge of this External Clock

$$\text{External Clock: } 1 \text{ MHz} < f_{\text{EXT}} < 180 \text{ MHz}$$

The active edge of the external clock is software

10 MHz Clock Reference

It is possible to generate the sampling clock based on a 10 MHz reference input. This is useful for RF systems that use a common 10 MHz reference clock.

ATS9462 uses an on-board PLL to generate the high frequency clock. Clock frequencies in the range of 150 MHz to 180 MHz can be generated with a 1 MHz resolution.

AUX Connector

ATS9462 provides an AUX (Auxiliary) BNC connector that is configured as a Trigger Output connector upon by default.

Software

ATS9462 is supplied with the powerful AlazarDSO software that allows the user to setup the acquisition hardware and capture, display and archive the signals.

A Windows compatible software development kit, ATS-SDK is also offered. It allows programs written in C/C++ and VisualBASIC to fully control the ATS9462.

A set of high performance VIs for LabVIEW 6.1 and higher, called ATS-VI, can also be purchased.

signal.

Input impedance for the External Clock input is fixed at 50 Ω . Input coupling for the external clock input is user-programmable between AC and DC coupling.

In order to operate the ADC under optimal conditions, the user must set the appropriate frequency range for the external clock being supplied. The following ranges are supported:

$$\text{Slow External Clock: } f_{\text{EXT}} < 1 \text{ MHz}$$

selectable between the rising or falling edge.

When configured as a Trigger Output, AUX BNC connector outputs a 5 Volt TTL signal synchronous to the ATS9462 Trigger signal, allowing user to synchronize their test systems to the ATS9462 Trigger.

When combined with the Trigger Delay feature of the ATS9462, this option is ideal for ultrasonic and other pulse-echo imaging applications.

Other uses of AUX connector include its use as a Trigger Enable Input and Clock Output.

Calibration

Every ATS9462 digitizer is factory calibrated to NIST-traceable standards. To recalibrate an ATS9462, the digitizer must either be shipped back to the factory or a qualified metrology lab.

A Linux based software development kit, ATS-Linux, is also available. Linux kernel versions up to v2.6 are supported.



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System Requirements

Personal computer with at least one free x4, x8 or x16 PCI Ex-press (v1.0a or v1.1) slot, 512 MB RAM, 100 MB of free hard disk space, SVGA

display adaptor and monitor with at least a 1024 x 768 resolution.

Power Requirements

+12V	1.2 A, typical
+3.3V	1.1 A, typical

Physical

Size	Single slot, half length PCI card (4.2 inches x 7.8 inches)
Weight	250 g

I/O Connectors

CH A, CH B, TRIG IN, AUX I/O ECLK	BNC female connectors SMA female connector
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Environmental

Operating temperature	0 to 55 degrees Celcius
Storage temperature	-20 to 70 degrees Celcius
Relative humidity	5 to 95%, non-condensing

Acquisition System

Resolution	16 bits
Bandwidth (-3dB)	
DC-coupled, 1M Ω	DC - 65 MHz
DC-coupled, 50 Ω	DC - 65 MHz
AC-coupled, 1M Ω	10 Hz - 65 MHz
AC-coupled, 50 Ω	100KHz - 65 MHz
Bandwidth flatness:	± 1 dB
Number of channels	2, simultaneously sampled
Maximum Sample Rate	180 MS/s single shot
Minimum Sample Rate	1 KS/s single shot for internal clocking
Full Scale Input ranges	
1 M Ω input impedance:	± 200 mV, ± 400 mV, ± 800 mV, ± 2 V, ± 4 V, ± 8 V, and ± 16 V, software selectable
50 Ω input impedance:	± 200 mV, ± 400 mV, ± 800 mV, ± 2 V, and ± 4 V, software selectable
DC accuracy	$\pm 2\%$ of full scale in all ranges
Input coupling	AC or DC, software selectable
Input impedance	50 Ω or 1M Ω $\pm 1\%$ in parallel with 50 pF ± 10 pF, software selectable
Input protection	
1M Ω	± 28 V (DC + peak AC for CH A, CH B and EXT only without exter nal attenuation)
50 Ω	± 4 V (DC + peak AC for CH A, CH B and EXT only without exter nal attenuation)

Amplifier Bypass Mode

Standard Feature	Yes
DIP Switch selectable	Yes, independently for each channel
Input Range	Approx. 550 mV rms
Input Coupling	DC, irrespective of the input coupling setting for the channel

Input Impedance	50 Ω , irrespective of the input impedance setting for the channel
Input bandwidth (-3dB)	85 MHz

Timebase System

Timebase options	Internal Clock or External Clock (Optional)
Internal Sample Rates	180 MS/s, 160 MS/s, 125 MS/s, 100 MS/s, 50 MS/s, 20 MS/s, 10 MS/s, 5 MS/s, 2 MS/s, 1 MS/s, 500 KS/s, 200 KS/s, 100KS/s, 50 KS/s, 20 KS/s, 10 KS/s, 5 KS/s, 2 KS/s, 1 KS/s
Internal Clock accuracy	± 2 ppm for 180MS/s & 160MS/s ± 25 ppm for 125 MS/s and lower

Dynamic Parameters

Typical values measured using a randomly selected ATS9462 with Amplifier Bypass Mode. Input was provided by a HP8656A signal generator, followed by a 9-pole, 1 MHz band-pass filter (TTE Q36T-1M-100K-50-720B). Input frequency was set at 1 MHz and output amplitude was 520 mV rms, which was approximately 95% of the full scale input.

SNR 72.9 dB
SINAD 72.3 dB
THD -83 dB
SFDR -82 dB

Note that these dynamic parameters may vary from one unit to another, with input frequency and with the full scale input range selected.

Optional ECLK (External Clock) Input

Signal Level ± 200 mV Sine wave or 3.3V LVTTTL Input impedance 50 Ω Maximum frequency 180 MHz for Fast External Clock 10 MHz for Slow External Clock Minimum frequency 1 MHz for Fast External Clock DC for Slow External Clock Decimation factor Software selectable from 1 to 100,000 Sampling Edge Rising or Falling, software selectable

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Optional 10 MHz Reference Input

Signal Level	± 200 mV Sine wave or 3.3V LVTTTL
Input impedance	50 Ω
Input Coupling	AC coupled
Input Frequency	10 MHz \pm 0.25 MHz
Sampling Clock Freq.	150 MHz to 180 MHz with 1 MHz resolution

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Triggering System

Mode	Edge triggering with hysteresis
Comparator Type	Digital comparators for internal (CH A, CHB) triggering and analog comparators for TRIG IN (External) triggering
Number of Trigger Engines	2
Trigger Engine Combination	OR, AND, XOR, selectable
Trigger Engine Source	CH A, CH B, EXT, Software or None, independently software selectable for each of the two Trigger Engines
Hysteresis	±5% of full scale input, typical
Trigger sensitivity	±10% of full scale input range. This implies that the trigger system may not trigger reliably if the input has an amplitude less than ±10% of full scale input range selected
Trigger level accuracy	±5%, typical, of full scale input range of the

TRIG OUT Output

Connector Used AUX Output Signal 5 Volt TTL Synchronization Synchronized to rising edge of sampling clock

	selected trigger source
Bandwidth	65 MHz
Trigger Delay	Software selectable from 0 to 9,999,999 sampling clock cycles
Trigger Timeout	Software selectable with a 10 us resolution. Maximum settable value is 3,600 seconds. Can also be disabled to wait indefinitely for a trigger event

TRIG IN (External Trigger) Input

Input impedance	1 MΩ in parallel with 50pF ±10pF
Bandwidth (-3dB)	DC-coupled DC - 25 MHz AC-coupled 10 Hz - 25 MHz
Input range	±5V or ±1V, software selectable
DC accuracy	±10% of full scale input
Input protection	±28V (DC + peak AC without external attenuation) Coupling AC or DC, software selectable

Install Disk

Certification and Compliances

CE Compliance

All specifications are subject to change without notice

ORDERING INFORMATION

ATS9462	ATS9462-001
ATS9462: External Clock Upgrade	ATS9462-004
C/C++, VB SDK for ATS9462	ATS9462-SDK
LabVIEW VI for ATS9462	ATS9462-VI
Linux Driver for ATS9462	ATS9462-LIN

ATS9462 ATS9462-001 ATS9462: External Clock Upgrade
ATS9462-004 C/C++, VB SDK for ATS9462 ATS9462-SDK
LabVIEW VI for ATS9462 ATS9462-VI Linux Driver for
ATS9462 ATS9462-LIN

Materials Supplied ATS9462 PCI Card
ATS9462 Hardware Manual ATS9462

北京迪阳世纪科技有限责任公司中国代理
010-62156134 62169728 www.pc17.com.cn

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